Customer No.: 31561
Application No.: 10/709,954
Docket No.: 11530-US-PA

In The Drawings:

Please substitute the attached amended drawing of Fig. 4C-4H for the pending drawing of Fig. 4C-4H.

REMARKS

Present Status of the Application

The drawings are objected to because the drawings fail to show that the conductive vias and the barrier layers are made of gold. The Office Action rejected claims 1-11 under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for the barrier layer and the conductive vias, does not reasonably provide enablement for both being made of a material such as gold. The Office Action rejected claims 1-7 and 9-11 under 35 U.S.C. 102(e), as being anticipated by Shimoto et al. (U.S. 6,861,757). The Office Action also rejected claims 1-4 and 6-11 under 35 U.S.C. 102(e), as being anticipated by Bohr (U.S. 6,617,681).

Applicants have amended the drawings, the title and the specification of the present application.

Applicants have also amended claims 1, 3 and 9 and canceled claim 2 to more clearly define the present invention.

Applicants further newly added claims 31-32. The limitations of claims 31-32 are shown in Figs. 4A-4H, and no new matter is entered.

After entry of the foregoing amendments, claims 1, 3-11 and 31-32 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Objections

The drawings are objected to because the drawings fail to show that the conductive vias and the barrier layers are made of gold. Applicants have amended FIGs.4C-4H, and the amended portion is adding the same hatches to the conductive vias and the barrier layers because the conductive vias and the barrier layers can be made of a material in an example.

The title of the invention "ELECTRICAL PACKAGE AND MANUFACTURING METHOD THEREOF" is amended to "ELECTRICAL PACKAGE CAPABLE OF INCREASING THE DENSITY OF BONDING PADS AND FINE CIRCUIT LINES INSIDE A INTERCONNECTION" that is clearly indicative of the invention to which the claims are directed.

Applicants further amended some typographic errors at paragraphs [0011], [0012], [0013], [0022], [0023], [0035] and [0037].

Rejection of 35 U.S.C. 112, first paragraph

The Office Action rejected claims 1-11 under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for the barrier layer and the conductive vias, does not reasonably provide enablement for both being made of a material such as gold. The Office Action points out how is the barrier layer 304a and the conductive vias 304b both fabricated using a conductive material such as gold?

Applicants explain the fabricating method of the barrier layer 304a and the conductive vias 304b as follows.

As shown in Fig. 4B, an isolating layer 322 having a plurality of openings 322a therein is formed over the support substrate 302. The openings 322a are via openings. Thereafter, as shown in Fig. 4C, a patterned barrier layer 304a and conductive vias 304b are formed over the support substrate 302. The barrier layer 304a is set up over the isolating layer 322 and the conductive vias 304b are set up inside the openings 322a. The barrier layer 304a and the conductive vias 304b can be formed by depositing a conductive layer (not shown in the drawing) over the insulating layer 322, wherein the conductive layer also fills the openings 322a, and then the conductive layer is patterned by using, for example, a lithography and etching process. Thereafter, the remained conductive layer forms the barrier layer 304a and the vias 304b. Thus, the barrier layer 304a and the vias 304b can be made from a material, such as gold. The conductive layer can also be other metallic material having good conductivity and etchant-resistant when etching support substrate. Because the barrier layer 304a and the vias 304b are fabricated from a metallic material, such as gold, they can prevent the inner circuits of the interconnection structure from damaging when the support substrate 302 is patterned subsequently (as shown in Fig. 4E) and provide good conductivity between the solder balls 320a, 320b and the bonding pads 308b (as shown in Fig. 4H).

Therefore, the barrier layer 304a and the conductive vias 304b can be fabricated using a conductive material such as gold. The fabricating method for forming the barrier layer 304a and

the conductive vias 304b as above mentioned is well known, and any person skilled in the art can understand.

Rejection of claims 1, 3-7 and 9-11 under 35 U.S.C. 102(e)

Applicants respectfully traverse the 102(e) rejection of claims 1, 3-7 and 9-11 because Shimoto et al. (U.S. 6,861,757) does not teach every element recited in these claims.

In order to properly anticipate Applicants' claimed invention under 35 U.S.C 102, each and every element of claim in issue must be found, "either expressly or inherently described, in a single prior art reference". "The identical invention must be shown in as complete details as is contained in the .... claim. Richardson v. Suzuki Motor Co., 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." See M.P.E.P. 2131, 8th ed., 2001.

The present invention is in general related an electrical package as claim 1 recites:

Claim 1. An electrical package comprising:
a multi-layer interconnection structure having a top surface, a bottom surface and an inner circuit therein, wherein the inner circuit has a plurality of bonding pads on the bottom surface of the multi-layer interconnection structure;
at least an electronic device positioned on the top surface of the multi-layer interconnection structure and electrically connected to the inner circuit of the multi-layer interconnection structure;
a support substrate made from a conductive material, wherein the support substrate is positioned on the bottom surface of the multi-layer interconnection structure, and ***the support substrate has a plurality of first openings, each first opening exposing one of the corresponding bonding pads***; and
an insulation layer covering the support substrate and exposing the bonding pads.

Shimoto fails to disclose, teach or suggest an insulation layer covering the support substrate and exposing the bonding pads. In Shimoto's reference, the structure, shown in Fig. 3 and Fig. 9, includes an insulating layer 6, an interconnection 8, electrodes 5, a supporting structure 16, a solder resist 17 and a chip 18. In particular, the solder resist 17 is set around the electrodes 5 (col. 9, lines 11-12). According to Fig. 3 showing, the solder resist 17 is disposed on the surface of the insulating layer 6 and between the solder balls 31. The solder resist 17 does not cover the supporting structure 16. However, the insulation layer of claim 1 covers the support substrate and exposes the bonding pads. Shimoto fails to disclose the support substrate is covered by an insulation layer.

In addition, at col. 19, lines 26-32, Shimoto discloses a prescribed region of the substrate 1 is selectively etched from the reverse surface side, and the electrodes 5 for making electrical connection with outside are made to be exposed and, at the same time, the substrate left along the periphery of the insulating layer 6 in the form of a frame is made to serve as a supporting structure 16. In other words, the supporting structure 16 is in the form of a frame. Thus, the supporting structure 16 just has one big opening exposing all of the electrodes 5. However, in claim 1 of the present application, the support substrate has a plurality of first openings, and each of the first openings exposes one of the corresponding bonding pads. Hence, Shimoto fails to teach or suggest the support substrate has a plurality of first openings, wherein each first opening exposes one of the corresponding bonding pads.

Shimoto also discloses by applying the solder resist 17 thereon, the solder balls 31 can be prevented from rolling when they are set, which makes their setting easier, and besides, once they are installed, the stress centralization on the contact sections between the solder balls and the electrodes 5 may be reduced, which raises the setting stability (col. 9, lines 15-20). However, the insulation layer of claim 1 covers the support substrate, and thus the insulation layer can be used to electrically isolate the support substrate from contacts if the contacts are disposed in the first openings to connect the bonding pads (the limitation "contacts" is recited in claim 6). The function and arrangement of the solder resist 17 are much different from the isolation layer as claim 1 recites.

For at least the foregoing reasons, Applicant respectfully submits that independent claim 1 patently defines over the prior art reference, and should be allowed. For at least the same reasons, dependent claims 3-7 and 9-11 patently define over the prior art as a matter of law, for at least the reason that these dependent claims contain all features of their respective independent claim.

Rejection of claims 1, 3-4 and 6-11 under 35 U.S.C. 102(e)

Applicants respectfully traverse the 102(e) rejection of claims 1, 3-4 and 6-11 because Bohr (U.S. 6,617,681) does not teach every element recited in these claims.

Bohr fails to disclose, teach or suggest that the support substrate is made from a conductive material. The structure (Fig. 1 and Fig. 3) disclosed by Bohr comprises a silicon die

102 and an OLGA package 104 including an insulating material 120, interconnects 118, a body portion 116, deep vias 122 and solder balls 110. In particular, the body portion 116 is a silicon substrate. Typically this silicon substrate is similar to the substrate used to produce integrated circuit die 102 (col. 5, line 65-col 6, lines 1). In other words, the body portion 116 is made form silicon which is a semiconductor material but not a conductive material. However, the support substrate of claim 1 is made from a conductive material. Because the support substrate of claim 1 is made from a conductive material, it can serve as the power plane or the ground plane of the electrical package and connections with the support substrate can be effected through contacts. Hence, electrical performance of the electrical package is improved.

For at least the foregoing reasons, Applicant respectfully submits that independent claim 1 patently defines over the prior art reference, and should be allowed. For at least the same reasons, dependent claims 3-4 and 6-11 patently define over the prior art as a matter of law, for at least the reason that these dependent claims contain all features of their respective independent claim.

Newly added claims 31-32

Applicants further newly added claims 31-32. The limitations of claims 31-32 are not disclosed by any one of Bohr and Shimoto.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,

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